## Claims

[c1] 1. A manufacturing method of a flash memory, comprising:
providing a substrate, on which a gate structure is formed;
forming a source region in the substrate at one side of the gate;
forming a first spacer on the sidewall of the gate structure;
forming a first conductive layer on the substrate;
forming a sacrificial layer on the first conductive layer;
removing portions of the sacrificial layer and the first conductive layer by a chemical mechanical polishing (CMP) method until the gate structure is exposed;
performing thermal oxidation to form a mask layer on the first conductive layer and the gate structure;
removing the sacrificial layer remaining on the first conductive layer;
using the mask layer as a mask to etch the first conductive layer until a square second conductive layer is formed;
removing the mask layer;
forming a lightly doped region in the substrate at the side where the second conductive layer is formed;
forming a second spacer on the sidewall of the second conductive layer; and
forming a drain region in the substrate at the side of the second conductive layer.

[c2] 2. The manufacturing method according to claim 1, wherein the gate structure comprises a tunneling oxide layer, a floating gate, a gate dielectric layer, a control gate and a gate cap layer.

[c3] 3. The manufacturing method according to claim 1, wherein the second conductive layer is formed as a select gate.

[c4] 4. The manufacturing method according to claim 2, wherein the material of the tunneling oxide layer includes silicon oxide.

[c5] 5. The manufacturing method according to claim 2, wherein the material of the gate dielectric layer includes silicon oxide/silicon nitride/oxide.

[c6] 6. The manufacturing method according to claim 1, wherein the material of the sacrificial layer includes silicon nitride.

[c7] 7. The manufacturing method according to claim 6, wherein the step of removing the sacrificial layer remaining on the first conductive layer includes wet etching.

[c8] 8. The manufacturing method according to claim 6, wherein the step of removing the sacrificial layer remaining on the first conductive layer includes using phosphoric acid as an etchant.

[c9] 9. The manufacturing method according to claim 1, wherein the material of the first spacer includes silicon oxide formed by chemical vapor deposition using tetra-ethyl-ortho-silicate and ozone as gas sources.

[c10] 10. The manufacturing method apparatus according to claim 1, wherein the second spacer includes silicon oxide formed by chemical vapor deposition using tetra-ethyl-ortho-silicate and ozone as gas sources.

[c11] 11. The manufacturing method according to claim 1, wherein the material of the first and second conductive layers includes doped polysilicon.

[c12] 12. A method for fabricating a square spacer, comprising:
providing a substrate having a stacked structure thereon;
forming a conductive layer on the substrate;
forming a sacrificial layer on the conductive layer;
removing portions of the sacrificial layer and the conductive layer until the stacked structure is exposed;
forming a mask layer on the conductive layer and the stacked structure;
removing the sacrificial layer remaining on the conductive layer; and
using the mask layer as a mask to etch the conductive layer, so as to form a square spacer.

[c13] 13. The method according to claim 12, wherein the step of removing portions of the sacrificial layer and the conductive layer includes chemical mechanical polishing.

[c14] 14. The method according to claim 12, wherein the material of the conductive layer includes doped polysilicon.

[c15] 15. The method according to claim 12, wherein the material of the sacrificial layer includes silicon nitride.

[c16] 16. The method according to claim 15, wherein the step of removing the sacrificial layer remaining on the conductive layer includes wet etching.

[c17] 17. The method according to claim 16, wherein the step of removing the conductive layer includes using phosphoric acid as etchant.

[c18] 18. The method according to claim 12, wherein the material of the mask layer comprises silicon oxide.

[c19] 19. The method according to claim 18, wherein the step of forming the mask layer includes thermal oxidation.

[c20] 20. The method according to claim 12, wherein the stacked structure includes a gate structure.